LISTING OF CLAIMS:

Claims 1-15 (canceled).

16. (Currently Amended) A method for testing an integrated circuit having a plurality of registers therein, each one of the registers including at least one register bit having a scan output, said method comprising ~~the steps of~~:

configuring the registers to form at least one serial shift register using the scan output of each register bit;

shifting a test pattern into the at least one serial shift register;

configuring the registers in a normal mode of operation, including disabling the scan output of at least some register bits so that for each of the at least some register bits, the scan output thereof is disabled from providing a value indicative of a value maintained by the register bit; and

applying at least one clock cycle to the registers.

17. (Currently Amended) The method of claim 16, wherein ~~the step of~~ configuring the registers in a normal mode of operation comprises ~~the step of~~ driving the scan output of at least some of the register bits to a predetermined logic value.

18. (Currently Amended) The method of claim 16, further comprising repeating ~~the steps of~~ configuring the registers to form at least one serial shift register chain, shifting,

configuring the registers in a normal mode of operation, and applying the at least one clock cycle for different test patterns a number of times.

19. (Currently Amended) The method of claim 18, further comprising, following ~~the step of~~ repeating ~~, the step of~~:

configuring the registers in a normal mode of operation, including disabling the scan output of the at least some register bits and driving the scan output to the predetermined logic value.

20. (Currently Amended) The ~~[[A]]~~ method of claim 16 wherein each register bit is configured as ~~for operating~~ a flip-flop having serial scan capabilities including a bit scan output, said method comprising ~~the steps of~~:

receiving a mode configuration signal for configuring the flip-flop between a test mode of operation and a normal mode of operation; and

selectively disabling the bit scan output from providing the logic value stored by the flip-flop based upon the value of the mode configuration signal received.

21. (Currently Amended) The method of claim 20, further comprising:

selectively driving the bit scan output to a predetermined logic value based upon the value of the mode configuration signal received.

22. (Currently Amended) The method of claim 21, wherein ~~the step of~~ driving comprises driving the bit scan output to a low logic value.

23. (Currently Amended) The method of claim 21, wherein ~~the step of~~ driving comprises driving the bit scan output to a high logic value.

24. (Currently Amended) The method ~~flip-flop~~ of claim 20, wherein the logic value stored in the flip-flop corresponds to an output of the flip-flop.

25. (Currently Amended) The method ~~flip-flop~~ of claim 20, wherein ~~the step of~~ selectively disabling is performed when said mode configuration signal configures the flip-flop in the normal mode of operation.

26. (New) A method for testing an integrated circuit, comprising:

selectively connecting a plurality of registers together to form at least one serial shift register when the integrated circuit is configured in a test mode of operation, each of the registers including at least one flip-flop, said at least one flip-flop within each of the registers including at least a test enable input, a scan input, a data input, a scan output and a data output;

enabling the at least one flip-flop in each of the registers for storing the signal appearing on the scan input of the at least one flip-flop and disabling from storing the signal appearing on the data input of the at least one flip-flop when the integrated circuit is in the test mode of operation;

disabling the at least one flip-flop in each of the registers from storing the signal appearing on the scan input of the at least one flip-flop and enabling for storing the signal appearing on the data input of the at least one flip-flop when the integrated circuit is in a normal mode of operation; and

enabling the at least one flip-flop in each of the registers to output a logic value stored by the at least one flip-flop on the scan output of the at least one flip-flop when in the test mode of operation and disabling from outputting on the scan output the logic value stored by the at least one flip-flop when in the normal mode of operation.

27. (New) A method for testing an integrated circuit comprising a register containing a plurality of register flip-flop bits, comprising:

receiving a test enable signal for configuring the integrated circuit between a test mode of operation and a normal mode of operation;

storing a data input from a data signal in each register flip-flop bit when the integrated circuit is in the normal mode of operation;

outputting data from each register flip-flop bit;

receiving a scan input test data signal for storage in the plurality of register flip-flop bits when the integrated circuit is in the test mode of operation;

enabling a scan output from the plurality of register flip-flop bits to output the logic values stored in the flip-flop bits when the integrated circuit is in the test mode of operation; and

disabling the scan output from outputting the logic values stored in the plurality of register flip-flop bits when the integrated circuit is in the normal mode of operation.